APPARATUS AND METHOD FOR PARALLEL PROGRAMMING OF ANTIFUSES

ABSTRACT OF THE DISCLOSURE

A method and apparatus for programming programmable elements of a plurality of memory devices in parallel. Each of the memory devices include an address latch for latching an address corresponding to a programmable element to be programmed and logic circuitry for receiving address load commands. The logic circuitry provides control signals to the address latch in response to receiving the load commands to cause the address latch to latch an corresponding to a programmable element to be programmed. By using the address latch and logic circuitry, the programming of a programmable element of a first memory device and the programming the second programmable element of a second memory device can occur in parallel.